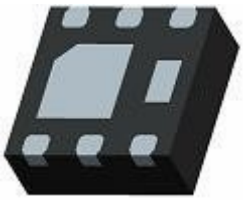
WPM1481

Single P-Channel, -12V, -5.5A, Power MOSFET

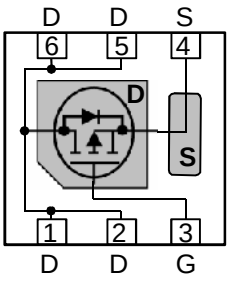
V_{DS} (V)	Typical Rds(on) (Ω)	I_D (A)
-12	0.022@ V_{GS}=−4.5V	-5.5
	0.030@ V_{GS}=−2.5V	-4.0
	0.045@ V_{GS}=−1.8V	-2.5



DFN2*2-6L

Descriptions

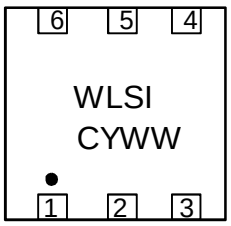
The WPM1481 is P-Channel enhancement MOS Field Effect Transistor. Uses advanced trench technology and design to provide excellent $R_{DS\ (ON)}$ with low gate charge. This device is suitable for use in DC-DC conversion, power switch and charging circuit. Standard Product WPM1481 is Pb-free.



Pin configuration (Top view)

Features

- Trench Technology
- Supper high density cell design
- Excellent ON resistance for higher DC current
- Extremely Low Threshold Voltage
- Small package DFN2*2-6L



WLSI = Company Code
C = Device Code
Y = Year
WW = Week

Marking

Applications

- Driver for Relay, Solenoid, Motor, LED etc.
- DC-DC converter circuit
- Power Switch
- Load Switch
- Charging

Order information

Device	Package	Shipping
WPM1481- 6/TR	DFN2*2-6L	3000/Reel&Tape

Absolute Maximum ratings

Parameter		Symbol	10 S	Steady State	Unit
Drain-Source Voltage		V_{DS}	-12		V
Gate-Source Voltage		V_{GS}	±12		
Continuous Drain Current [a d]	T_A=25°C	I_D	-5.1	-4.3	A
	T_A=70°C		-4.0	-3.4	
Maximum Power Dissipation [a d]	T_A=25°C	P_D	1.9	1.4	W
	T_A=70°C		1.2	0.9	
Continuous Drain Current [b d]	T_A=25°C	I_D	-3.7	-3.0	A
	T_A=70°C		-3.0	-2.4	
Maximum Power Dissipation [b d]	T_A=25°C	P_D	1.0	0.6	W
	T_A=70°C		0.6	0.4	
Pulsed Drain Current [c]		I_{DM}	-24		A
Operating Junction Temperature		T_J	-55~150		°C
Lead Temperature		T_L	260		°C
Storage Temperature Range		T_{stg}	-55 ~150		°C

Thermal resistance ratings

Parameter		Symbol	Typical	Maximum	Unit
Junction-to-Ambient Thermal Resistance [a]	t ≤ 10 s	$R_{\theta JA}$	49	64	°C/W
	Steady State		66	88	
Junction-to-Ambient Thermal Resistance [b]	t ≤ 10 s	$R_{\theta JA}$	84	118	
	Steady State		125	180	
Junction-to-Case Thermal Resistance	Steady State	$R_{\theta JC}$	32	42	

a Surface mounted on FR-4 Board using 1 square inch pad size, 1oz copper

b Surface mounted on FR-4 board using minimum pad size, 1oz copper

c Pulse width<380μs, Single pulse

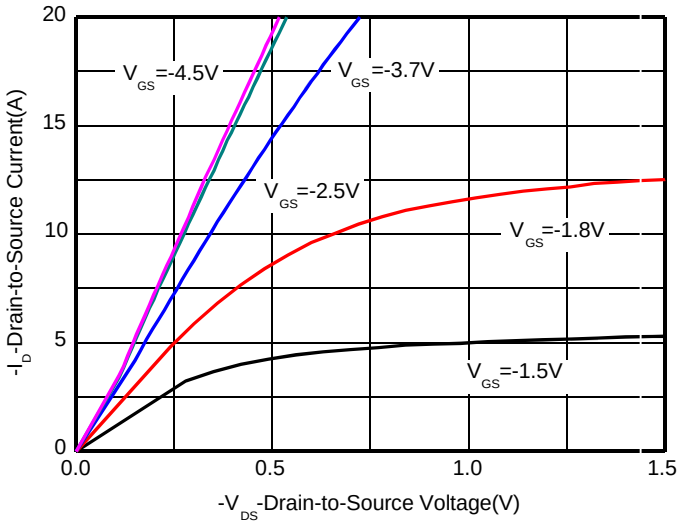
d Maximum junction temperature T_J=150°C.

e Pulse test: Pulse width <380 us duty cycle <2%.

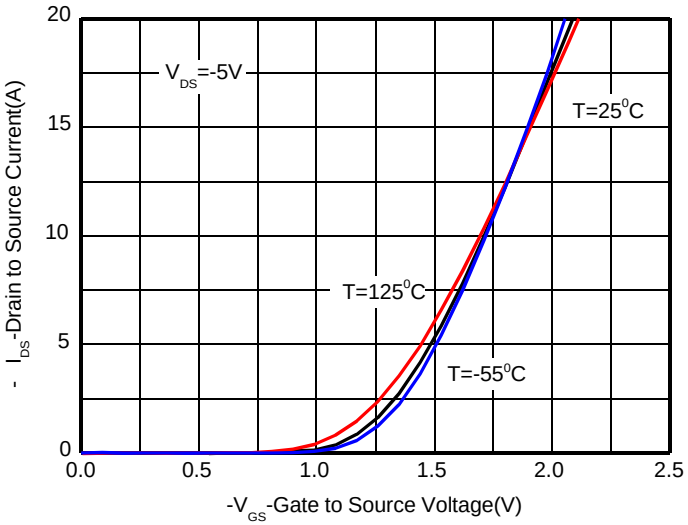
Electronics Characteristics (Ta=25°C, unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-to-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0 V, I_D = -250uA	-12			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -10V, V_{GS} = 0V			-1	uA
Gate-to-source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} =±10V			±100	nA
ON CHARACTERISTICS						
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = -250uA	-0.4		-0.9	V
Drain-to-source On-resistance [b, e]	$R_{DS(on)}$	V_{GS} = -4.5V, I_D = -5.5A		22	26	mΩ
		V_{GS} = -2.5V, I_D = -4.0A		30	38	
		V_{GS} = -1.8V, I_D = -2.5A		45	59	
Forward Transconductance [e]	g_{FS}	V_{DS} =-5.0V, I_D = -5.5A		23		S
CAPACITANCES, CHARGES						
Input Capacitance	C_{ISS}	V_{GS} = 0 V,		1880		pF
Output Capacitance	C_{OSS}	f = 1.0 MHz,		437		
Reverse Transfer Capacitance	C_{RSS}	V_{DS} = -10 V		413		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = -4.5 V, V_{DS} = -10 V, I_D = -5.5A		44.5		nC
Threshold Gate Charge	$Q_{G(TH)}$			3.5		
Gate-to-Source Charge	Q_{GS}			1.7		
Gate-to-Drain Charge	Q_{GD}			9.25		
SWITCHING CHARACTERISTICS						
Turn-On Delay Time	$td_{(ON)}$	V_{GS} = -4.5 V, V_{DS} = -6 V, R_L=3 Ω, R_G=6 Ω		33.6		ns
Rise Time	tr			35.6		
Turn-Off Delay Time	$td_{(OFF)}$			50		
Fall Time	tf			63		
BODY DIODE CHARACTERISTICS						
Forward Voltage	V_{SD}	V_{GS} = 0 V, I_S = 1.0A		-0.76	-1.5	V

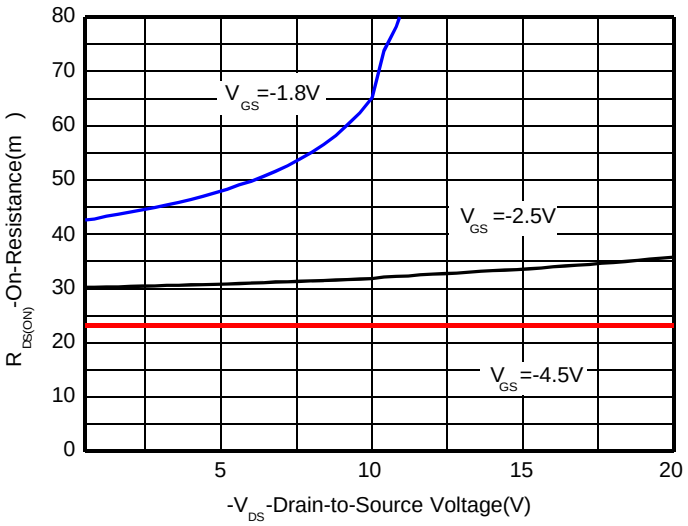
Typical Characteristics (Ta=25°C, unless otherwise noted)



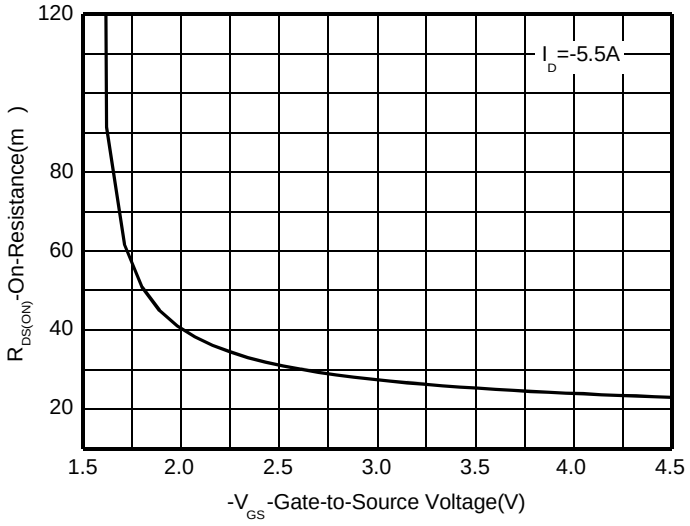
Output characteristics



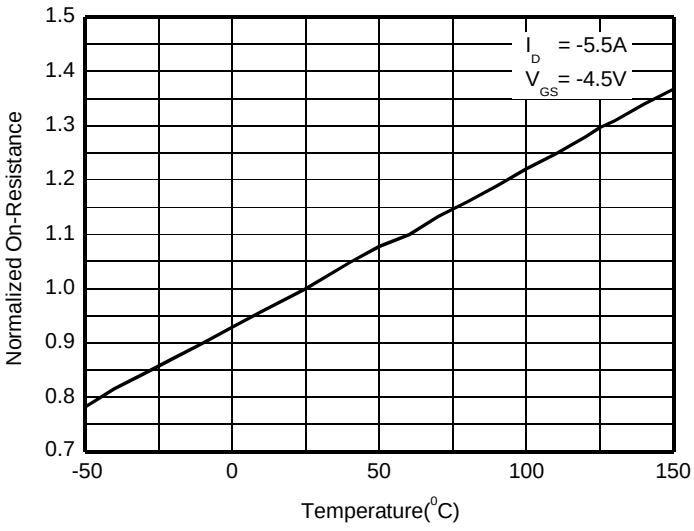
Transfer characteristics



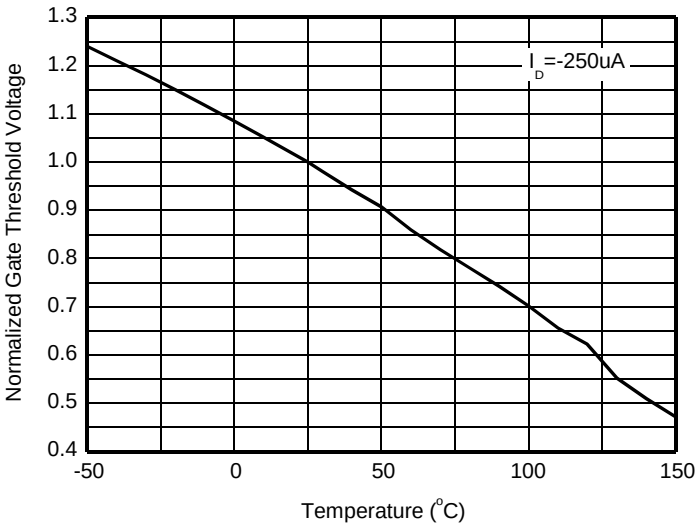
On-Resistance vs. Drain current



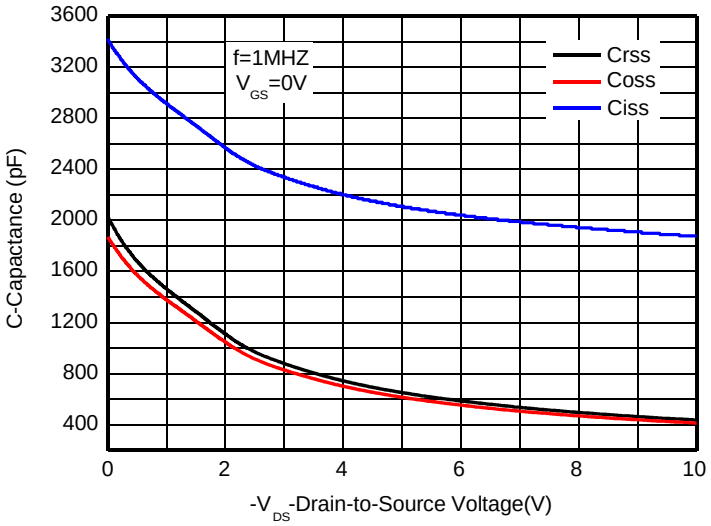
On-Resistance vs. Gate-to-Source voltage



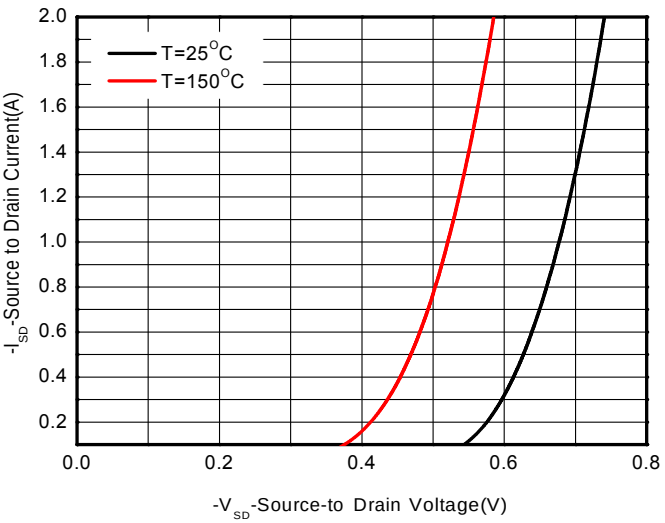
On-Resistance vs. Junction temperature



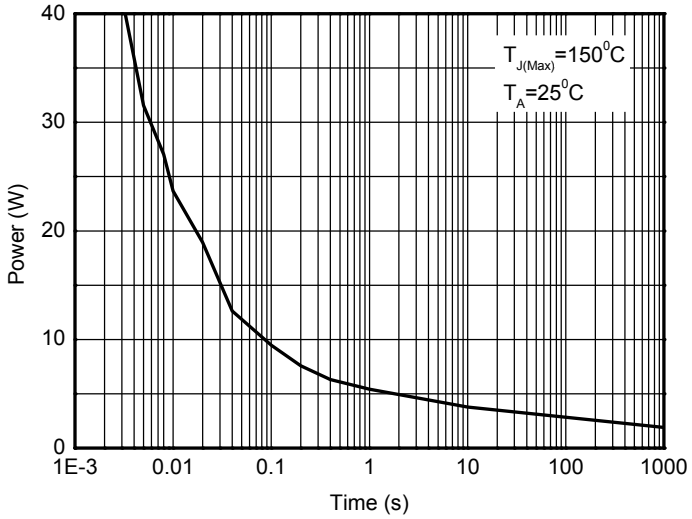
Threshold voltage vs. Temperature



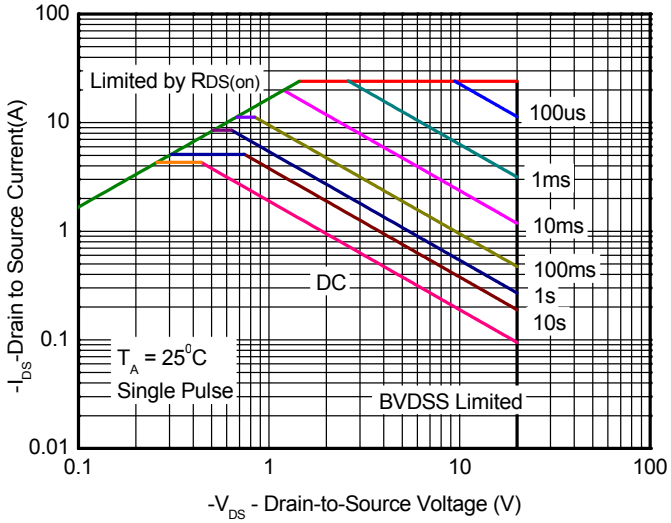
Capacitance



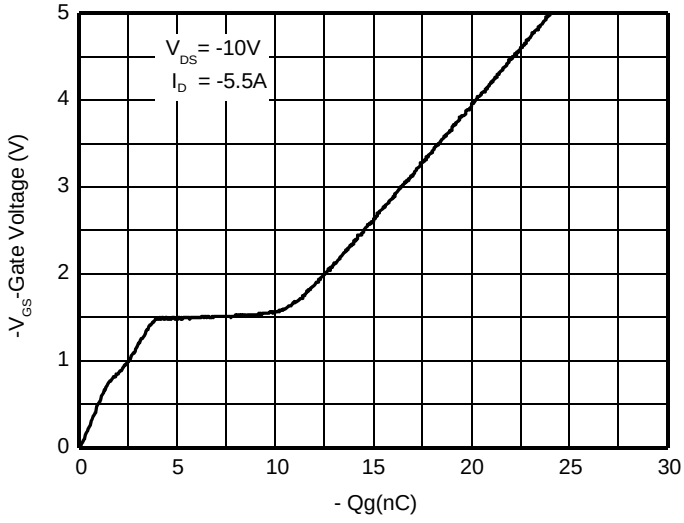
Body diode forward voltage



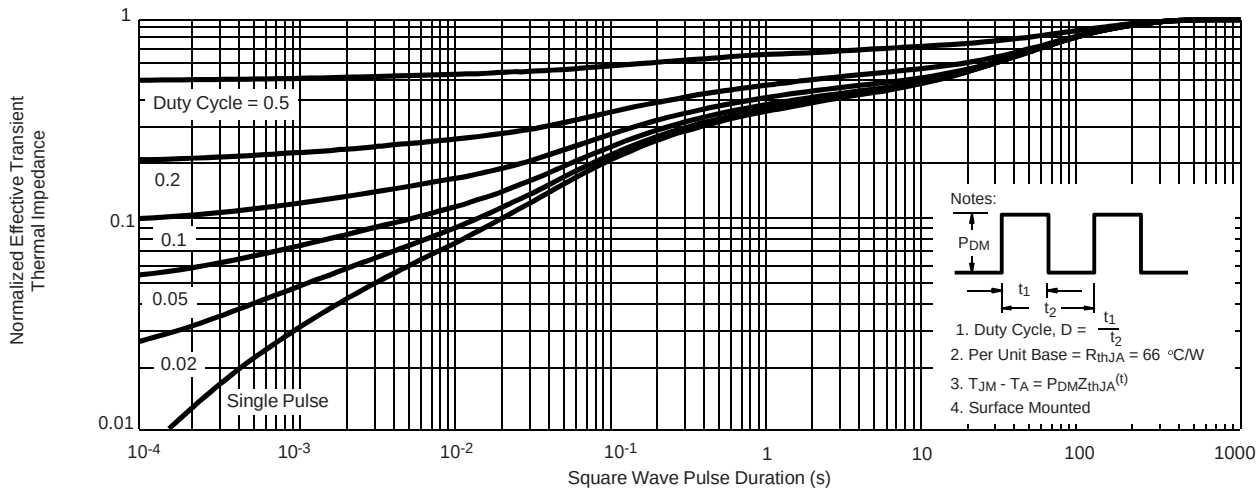
Single pulse power



Safe operating power



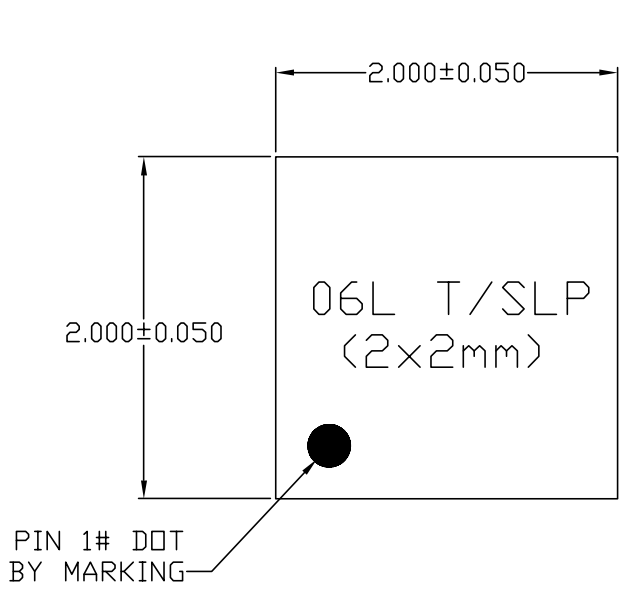
Gate Charge Characteristics



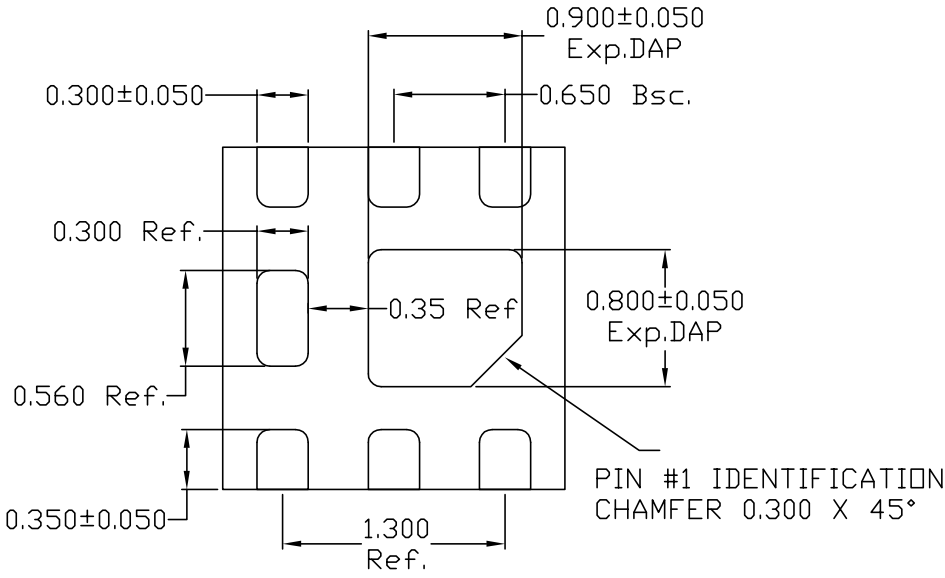
Transient thermal response (Junction-to-Ambient)

Package outline dimensions

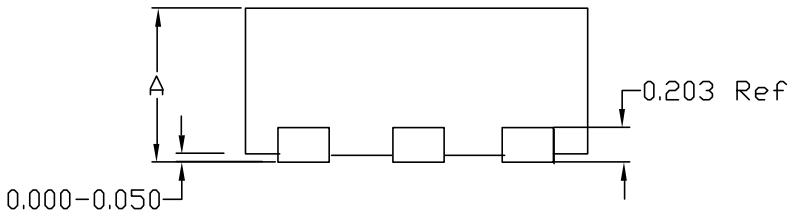
DFN2*2-6L



Top view



Bottom view



Side View

NOTE:

1) TSLP AND SLP SHARE THE SAME EXPOSE OUTLINE BUT WITH DIFFERENT THICKNESS:

		TSLP	SLP
A	MAX.	0.800	0.900
	NOM.	0.750	0.850
	MIN.	0.700	0.800