MP3422

6.5A, 600kHz Synchronous Step-up Converter with Output Disconnect

The Future of Analog IC Technology

PRELIMINARY SPECIFICATIONS SUBJECT TO CHANGE

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DESCRIPTION

The MP3422 is a high-efficiency, synchronous, current–mode, step-up converter with output disconnect.

The MP3422 can start up from an input voltage as low as 2.5V while provide inrush current limiting, and output short-circuit protection. The integrated, P-channel, synchronous rectifier improves efficiency and eliminates the need for an external Schottky diode. The PMOS disconnects the output from the input when the part shuts down.

The 600kHz switching frequency allows for small external components, while the internal compensation and the soft-start minimize the external component count. MP3422 provides small size solution for 5V/2.5A load from a supply voltage down to 2.8V.

The MP3422 is available in 14-pin QFN 2mmx2mm package.

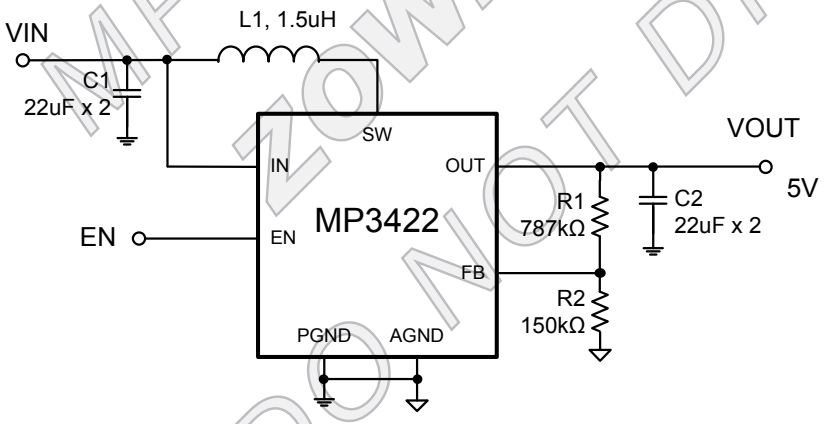
FEATURES

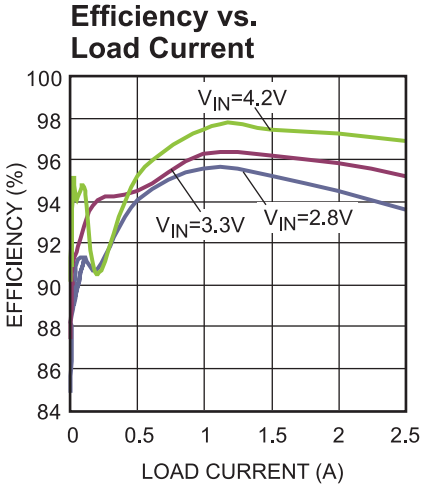
- 2.5V to 5.5V Input Work Range
- 2.5V to 5.5V Output Range
- Internal Synchronous Rectifier
- 600kHz Fixed Frequency Switching
- >6.5A Switch Current Limit Capability
- 43uA Quiescent Current
- High Efficiency over Full Load Range
- Internal Soft-start and Compensation
- True Output Load Disconnect from Input
- OCP, SCP, OVP and OTP Protection
- Small QFN2x2-14 Package

APPLICATIONS

- Battery-Powered Products
- Personal Medical Devices
- Portable Media Players
- Wireless Peripherals
- Handheld Computers and Smartphones

TYPICAL APPLICATION



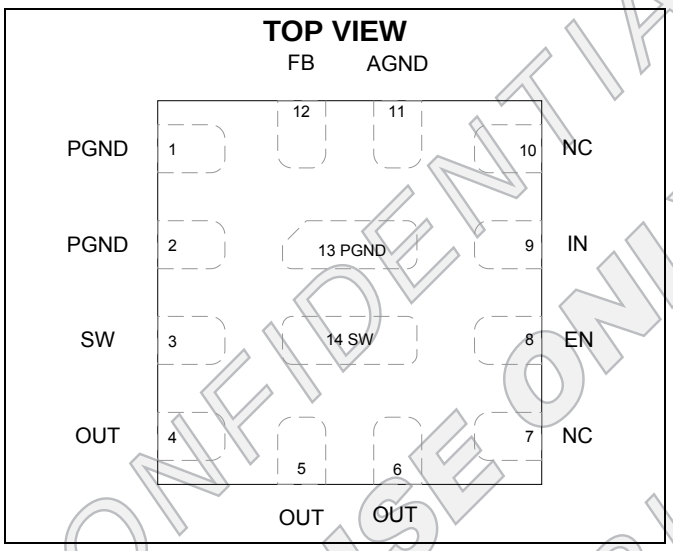


ORDERING INFORMATION

Part Number*	Package	Top Marking
MP3422GG	QFN-14 (2mmX2mm)	CN

* For Tape & Reel, add suffix –Z (e.g. MP3422GG–Z)

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS (1)

SW Pin .....-0.3V to +6.5V (9V for <5ns)
All other Pins ..... -0.3V to +6.5V
Continuous Power Dissipation (T_A = +25°C) (2)
.....1.56W
Junction Temperature.....150°C
Lead Temperature ..... 260°C
Storage Temperature..... -65°C to +150°C

Recommended Operating Conditions (3)

Supply Voltage V_{IN} ..... 2.5V to 5.5V
V_{OUT} ..... 2.5V to 5.5V
Operating Junction Temp. (T_J). -40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

QFN14 (2mmx2mm)..... 80..... 16 °C/W

Notes:
1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = V_{EN} = 3.3V, V_{OUT} = 5V, T_J = 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Voltage Range						
Operating Input Voltage	V_{IN}		2.5		5.5	V
Quiescent Current	I_{Q_NS}	V_{EN}=V_{IN}=3.3V, V_{OUT}=5V, no load Measured on OUT pin		43		μA
		V_{EN}=V_{IN}=3.3V, V_{OUT}=5V, no load Measured on IN pin		0.3		μA
Shutdown Current	I_{SD}	V_{EN}=V_{OUT}=0V, Measured on IN pin		0.1		μA
IN UVLO Rising Threshold	$V_{UVLO\ IN-R}$	V_{IN} Rising		1.3		V
IN UVLO Falling Threshold	$V_{UVLO\ IN-F}$	V_{IN} Falling, V_{OUT}=5V		800		mV
VOUT UVLO Falling Threshold	$V_{UVLO\ OUT-F}$	V_{OUT} Falling, V_{IN}=3.3V		1.7		V
Step-up Converter						
Operation Frequency	V_{SW}		500	600	700	kHz
Feedback Voltage	V_{FB}		795	807	819	mV
Feedback Input Current	I_{FB}	V_{FB}=850mV		1	50	nA
NMOS On-Resistance	$R_{NDS\ ON}$			13		mΩ
NMOS Leakage Current	$I_{N\ LK}$	V_{SW}=5V		0.1		μA
PMOS On-Resistance	$R_{PDS\ ON}$			18		mΩ
PMOS Leakage Current	$I_{P\ LK}$	V_{SW}=5V, V_{OUT}=0V		0.1		μA
Maximum Duty Cycle	D_{MAX}		90	95		%
Linear Charge Current Limit(5)	I_{CH_LIMIT}	Vo=1.7		0.7		A
		Vo=0		0.2		A
NMOS Current Limit(5)	$I_{SW\ LIMIT1}$	V_{IN}=5V, V_{OUT}=3.3V		4		A
	$I_{SW\ LIMIT2}$	Duty=44%, Vin=2.8V, Vo=5V	6.5			A
Logic Interface						
EN High-Level Threshold	$V_{EN\ H}$	Rising	1.2			V
EN Low-Level Threshold	$V_{EN\ L}$	Falling			0.4	V
EN Input Current	I_{EN}	Connect to V_{IN}		10		nA
Protection						
Thermal Shutdown(5)				150		°C
Over Temperature Hysteresis(5)				20		°C

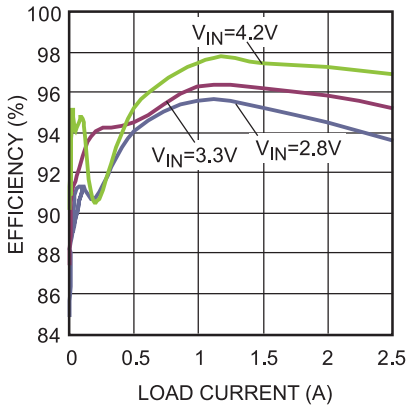
Notes:

5) Guaranteed by characterization, not production tested

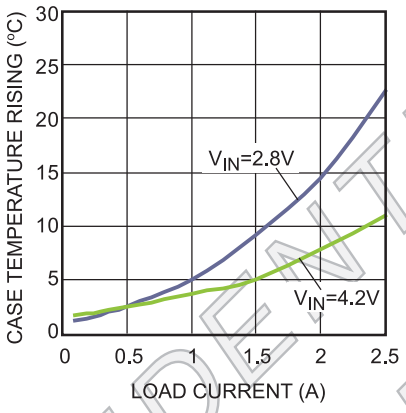
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 3.3V, V_{OUT} = 5V, L=1.5uH, T_A = 25°C, unless otherwise noted.

Efficiency vs. Load Current

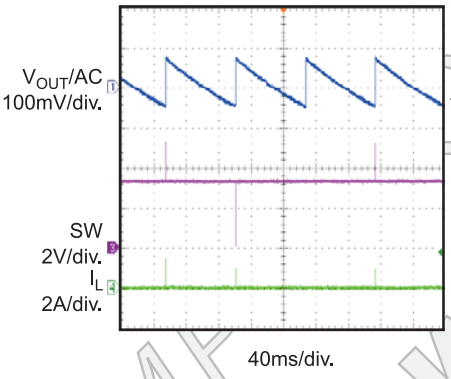


Case Temperature Rising vs. Load Current



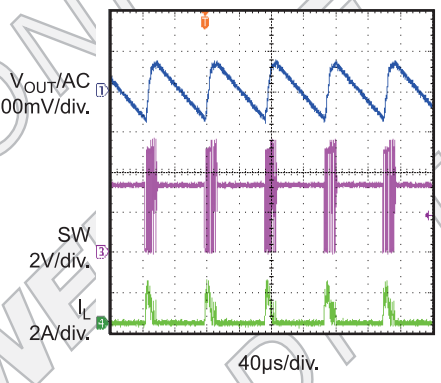
Output Voltage Ripple

Load = 0A



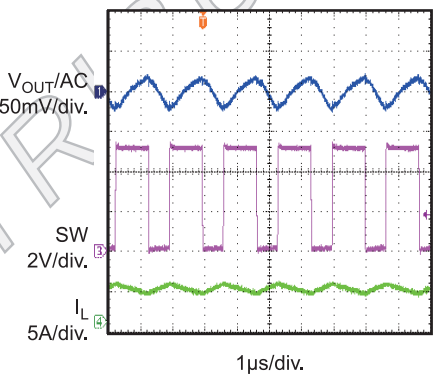
Output Voltage Ripple

Load = 0.1A



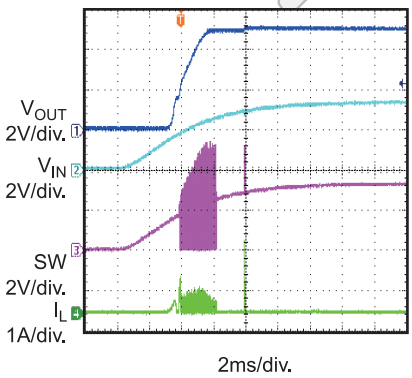
Output Voltage Ripple

Load = 2.5A



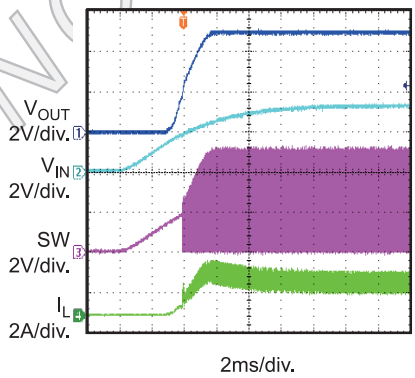
V_{IN} Startup

Load = 0A



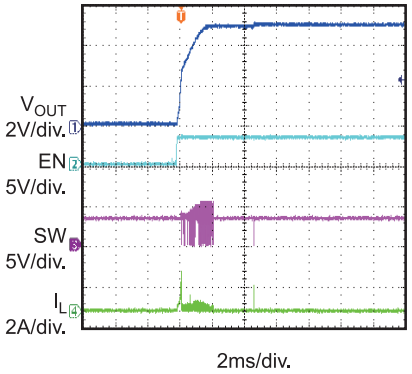
V_{IN} Startup

Load = 5Ω



EN Start up

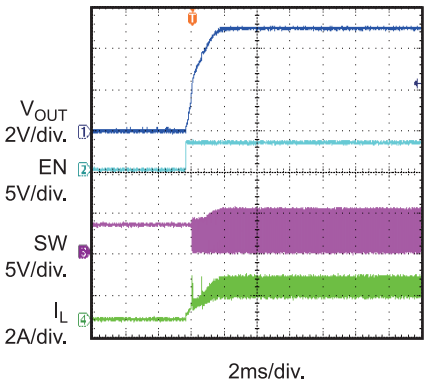
Load = 0A



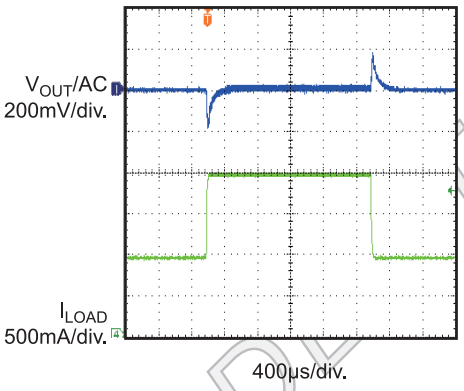
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 3.3V, V_{OUT} = 5V, L=1.5uH, T_A = 25°C, unless otherwise noted.

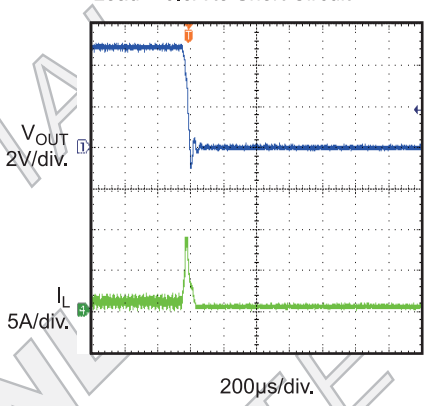
EN Startup
Load = 5Ω



Load Transient
Load = 1A <--> 2A at 50mA/µs



Short Circuit
Load = 0.5A to Short Circuit



PIN FUNCTIONS

Pin #	Name	Pin Function
1, 2, 13	PGND	Power Ground.
3, 14	SW	Power Switch Output. SW is the connection node of the internal NMOS switch and synchronous switch. Connect the power inductor between SW and input power. Keep these PCB trace lengths as short and wide as possible to reduce EMI and voltage spike.
4, 5, 6	OUT	Output Pin. OUT is the drain of the Internal Synchronous Rectifier MOSFET. Bias is derived from OUT when V_{OUT} is higher than V_{IN}. PCB trace length from OUT to the output filter capacitor(s) should be as short and wide as possible. OUT is completely disconnected from IN when EN is low due to the output disconnect feature.
7	NC	No Connect. Reserve for factory use only, float or connect this pin to GND in application.
8	EN	Chip Enable Control Input.
9	IN	Power Supply Input. The device gets its startup bias from IN. Must be locally bypassed. Once OUT exceeds IN, bias comes from OUT. Thus, once started, operation is completely independent from IN.
10	NC	No Connect. Reserve for factory use only, must be connected to IN pin in application.
11	AGND	Analog Signal Ground.
12	FB	Feedback Input to Error Amplifier. Connect resistor divider tap to this pin. The output voltage can be adjusted from 2.5V to 5.5V

FUNCTION DIAGRAM

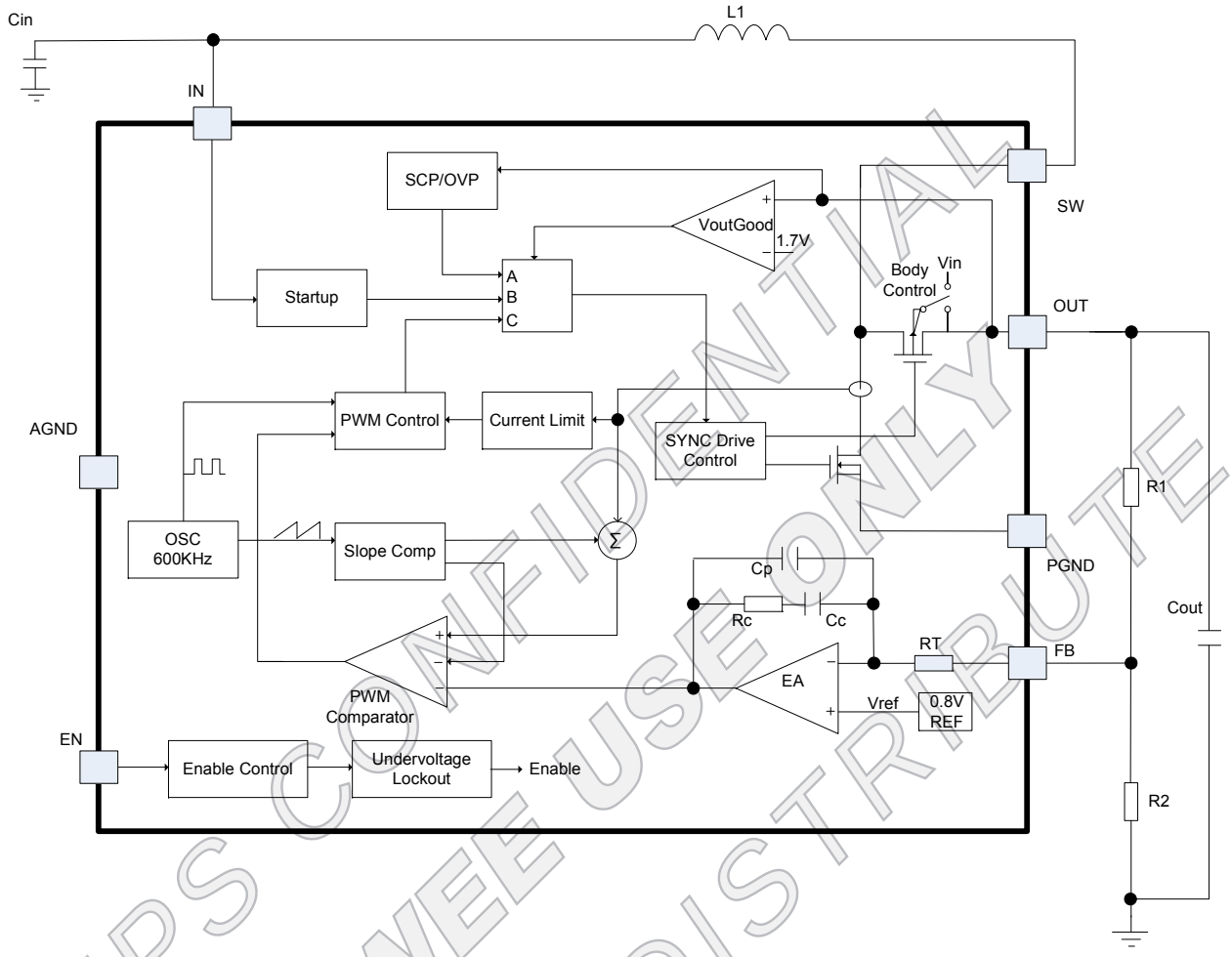


Figure 1: Functional Block Diagram

OPERATION

The MP3422 is a 600kHz, synchronous, step-up converter housed in a QFN2x2-14 package with true output disconnect. The device features fixed-frequency current-mode PWM control for exceptional line and load regulation. Internal soft-start and loop compensation simplify the design process and minimize the external components. The internal low-$R_{DS(ON)}$ MOSFETs combined with frequency stretching operation enable the device to maintain high efficiency over a wide current-load range.

Start-Up

When IC is enabled, MP3422 starts up with linear charge period. During linear charge period, the rectifier PMOS turns on until the output capacitor is charged to 1.7V. The PMOS current is limited to 0.2A when V_{OUT} is 0V to avoid inrush current. While the output ramps up, the PMOS current limit increases and finally reaches to 0.7A at 1.7V output voltage condition. This circuit also helps to limit the output current under short circuit condition.

Once output is charged to 1.7V, linear charge period elapses and MP3422 starts switching with normal close loop operation. The V_{OUT} starts to rise to higher than 1.7V under internal soft-start control. In normal operation, MP3422 works in down mode with 4A typical peak current limit while Vo is lower than Vin+0.3V, and works in boost mode once Vo is higher than Vin+0.3V with more than 6.5A current limit. .

Once the output voltage exceeds input voltage, MP3422 powers internal circuits from V_{OUT} instead of V_{IN}.

Soft-Start

The MP3422 provides soft-start by charging an internal capacitor with a current source. The internal soft start does not take charge and keep rising follow FB during linear charge period. Once linear charge elapse, the voltage on this capacitor is charged, in turn, slowly ramps up the reference voltage. The reference soft-start time is typically 2ms from 0V to 0.8V. The soft-start capacitor is discharged completely in the event of a commanded shutdown, thermal shutdown or short circuit at the output.

Device Enable

The device is put into operation when EN is set high. It is put into a shutdown mode when EN is set to GND. In shutdown mode, the regulator stops switching, all internal control circuitry is switched off, and the load is isolated from the input.

Power Save Mode

The MP3422 will automatically enter power save mode (PSM) when load decreases, and goes back to PWM mode when load increases. In PSM, the converter will stretch down the frequency firstly to save switching loss and driver loss. MP3422 subjects to pulse skip mode if load continue decrease.

Error Amplifier

The error amplifier (EA) is an internally-compensated amplifier. The EA compares the internal 0.807V reference voltage against V_{FB} to generate an error signal. The output voltage of MP3422 could be adjusted by external resistor divider. A voltage divider from V_{OUT} to ground programs the output voltage via FB from 2.5V to 5.5V using the equation:

$$Vout=0.807V \times (1+R1/R2)$$

The value of R1 and R2 should be set as large as desired to achieve a low quiescent current. Usually, a value of R1 larger than 250kΩ is preferred for a good stability and transient balance.

Current Sensing

Lossless current sensing converts the NMOS switch current signal to a voltage to be summed with the internal slope compensation. The summed signal is compared to the error amplifier output to provide a peak current control command for the PWM. Minimum peak switch current limite is 6.5A. The switch current signal is blanked for 60ns internally to enhance noise rejection.

Output Disconnect

The MP3422 is designed to allow true output disconnect by eliminating body diode conduction of the internal PMOS rectifier. This allows V_{OUT} go to zero volts during shutdown, or allows V_{IN} go to zero volts during shutdown but V_{OUT} is biased. It also allows for inrush current limit at start-up, minimizing surge current seen by the input supply. Note that to obtain the advantage of output disconnect, there must not be an external Schottky diode connected between the switch pin and V_{OUT}.

Over Load and Short Circuit Protection

When over load or short circuit occurs, the output voltage will drop. If V_{OUT} drops below Vin+0.3V, MP3422 will run back into down mode and run into linear charge mode when Vout drops below 1.7V. If Vout drops to lower than 70% of nominal output voltage, MP3422 will shut down immediately and re-start after 50us as a new power-on cycle.

Over Voltage Protection

If voltage on OUT pin is higher than 7V, the boost switching will stop. It can help protect internal power MOSFET from over voltage stress. After output drops to lower than 7V, the switching will recover automatically.

Thermal Shutdown

The device has an internal temperature monitor if the die temperature exceeds 150°C, the switches turn off. Once the temperature drops below 130°C, it will turn on again.

APPLICATION INFORMATION

COMPONENT SELECTION

Input Capacitor Selection

Low ESR input capacitors reduce input switching noise and reduce the peak current drawn from the battery. Ceramic capacitors are a good choice for input decoupling and should be located as close as possible to the device. A ceramic capacitor larger than 22μF is recommended to restrain V_{IN} ripple.

Output Capacitor Selection

The output capacitor requires a minimum capacitance value of 22μF at the programmed output voltage to ensure stability over the full operating range. A higher capacitance value may be required to lower the output ripple and also the transient response. Low ESR capacitors such as X5R or X7R type ceramic capacitors are recommended. Supposing that ESR is zero, the minimum output capacitor to support the ripple in the PWM mode could be calculated by:

$$C_O \geq \frac{I_O \times (V_{OUT(MAX)} - V_{IN(MIN)})}{f_S \times V_{OUT(MAX)} \times \Delta V}$$

Where,
$V_{OUT(MAX)}$ = Maximum output voltage
$V_{IN(MIN)}$ = Minimum Input voltage
I_O=Output current
f_S = Switching frequency
ΔV= Acceptable output ripple
1μF small size ceramic capacitor is recommended to place between OUT pin and PGND pins, which can reduce spikes on the SW node and improve EMI performance.

Inductor Selection

The MP3422 can apply small surface mount chip inductors due to its 600kHz switching frequency. Inductor values between 1μH and 2.2μH are suitable for most applications. Larger values of inductance will allow slightly greater output current capability by reducing the inductor ripple current, but larger value inductance increases component size. The minimum inductance value is given by:

$$L \geq \frac{V_{IN(MIN)} \times (V_{OUT(MAX)} - V_{IN(MIN)})}{2 \times V_{OUT(MAX)} \times \Delta I_L \times f_S} \quad (3)$$

ΔI_L=Acceptable inductor current ripple

The inductor current ripple is typically set for 30% to 40% of the maximum inductor current. The inductor should have low DCR (series resistance of the inductor current without saturating windings) to reduce the resistive power loss. The saturated current (I_{SAT}) should be large enough to support the peak current.

PCB Layout Considerations

For switching power supplies with high switching frequency, the layout is always an important step in design. A poor layout would result in reduced performance, EMI problems, resistive loss and even system instability. Following step would help to guarantee a good layout design:

1. Output capacitor must be placed as close as possible from V_{OUT} pin to PGND pin. A small size decoupling capacitor (>100nF) is recommended parallel with bulk output capacitor and close to IC. This is very important to reduce the spike on the SW node and also gets a better EMI performance.
2. Input capacitor, and inductor should be placed close to the IC, SW trice should be as possible as short and wide.
3. Feedback loop should be far away from noise source such as SW trace, the feedback divider resistor should be as close as possible to FB and AGND pin.
4. The ground return of input/output capacitor should be tied close to the PGND pin with large GND copper area, vias around GND pin is recommended to lower the die temperature
5. For NC pin layout, pin 10 must be connected to IN and pin 7 can be float or connected to GND.

Figure 2 shows the recommended components place for MP3422.

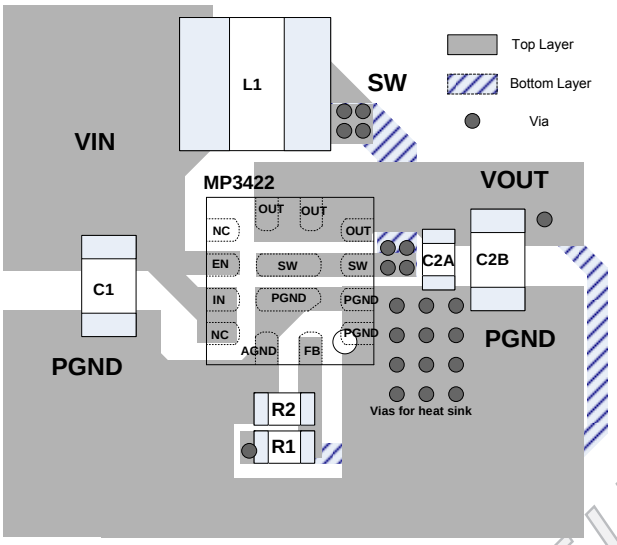


Figure 2, Layout Recommendation

Design Example

Below is a design example following the application guidelines for the following specifications:

Table 1, Design Example

V_{IN}	2.8V-4.2V
V_{OUT}	5V
I_{OUT}	0A-2.5A

The typical application circuit for V_{OUT} = 5V in Figure 3 shows the detailed application schematic, and is the basis for the typical performance waveforms. For more detailed device applications, please refer to the related Evaluation Board Datasheets.

TYPICAL APPLICATION CIRCUITS

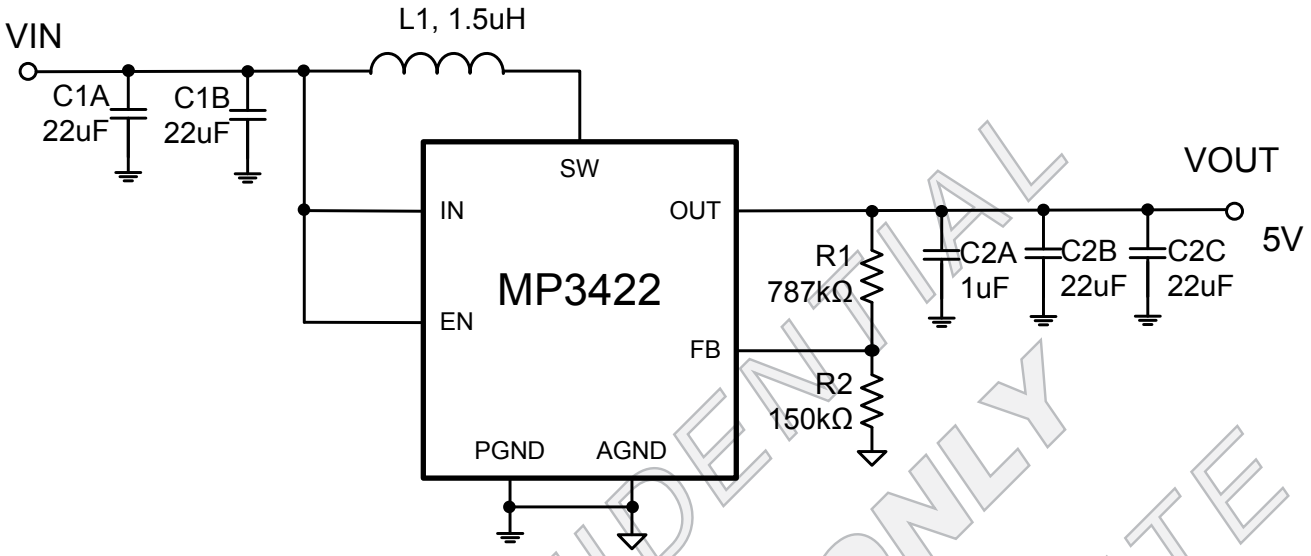
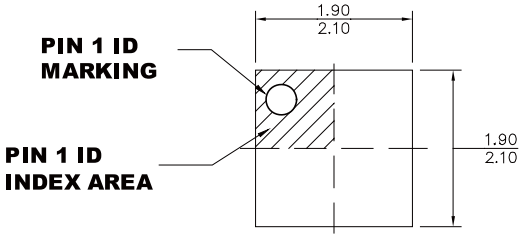


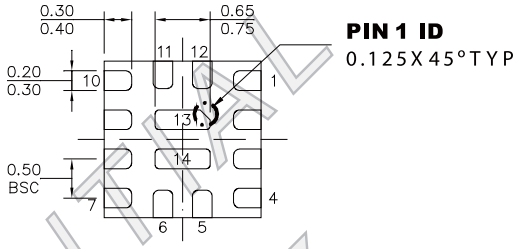
Figure 3, Typical Boost Application Circuit, V_{IN}=2.8V to 4.2V, V_O=5V

PACKAGE INFORMATION

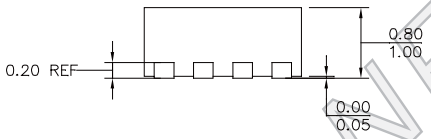
QFN14 (2mmX2mm)



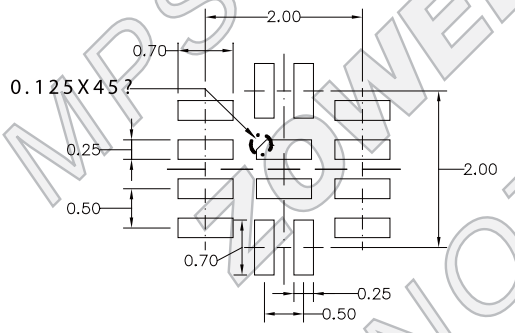
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.